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**EE314 – Mini-Project**

**Task B: Filter & Decimator**

**Group 8**

**GROUP: Group B DATE: 21/04/2023**

*I declare that I have not plagiarised or excessively quoted the work of others, nor have I colluded*

*with others to represent collaborative work as my own. I have appropriately cited all information*

*derived from the published and unpublished work of other and less then 5% of my submission*

*quotes the source material directly.*

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# Project Completion Plan:

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| Tasks | Description | Name |
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# Introduction (~ 1 page):

## Block Diagram

DUT

in

IN

out

rst

OUT

RST

CLK

clk

## Description of the use of such a module in everyday systems

Decimation is used in applications where the Nyquist frequency of a signal is a lot larger than the highest frequency in the signal, helping to get rid of unnecessary data and reduce the required sampling frequency for the signal. In turn reducing the required computational power for processing the signal. Decimators can also reduce noise, improving the signal to noise ratio.

# Verilog Testbench (with Comments):

Code + Comments

# Verilog Module(s) (with Comments):

Code + Comments

# Description of the Design

Describe the functionality of the design in your own words.

# Simulated Results

Indicate examples or sections of signals from a testbench simulation which clearly demonstrate the module(s) work as expected.

# Conclusions

## Explain in words how you validated that the design works correctly, and how it is possible to tell that it works.

## What additional features if any did you incorporate into the design or testbench to improve it?

## What are the limitations of your design?